ABSTRACT OF THE DISCLOSURE

A processor and method capable of executing conditional instructions is disclosed, which can execute an instruction set including M-bit instructions and N-bit instructions. The instruction set has condition execution instructions and M-bit parallel condition execution instructions. Each parallel condition execution instruction has a first and a second N-bit instruction. An instruction fetching device fetches at least one instruction to be performed. An instruction decoder decodes the instruction fetched by the instruction fetching device. An instruction executing device executes the instruction outputted by the instruction decoder, wherein a flag is set according to a result of executing a condition execution instruction. A mode switching device switches the instruction decoder to decode one of the first and the second N-bit instructions according to the state of the flag, so as to be subsequently performed by the instruction executing device, when a parallel condition execution instruction is fetched.